CLAIMS

1. A method for altering the semiconductor characteristics of a semiconductor element, the method comprising directing an energy beam at the semiconductor element, wherein the energy beam is substantially absorbed by a first portion of the semiconductor element.

2. The method of Claim 1, wherein the energy beam is produced by a CO_2 laser.

3. The method of Claim 1, wherein the energy beam is produced by a YAG laser.

4. The method of Claim 3, wherein the energy beam has a wavelength of greater than 1.2 μm.

5. The method of Claim 1, wherein the energy beam is produced by a laser ablation system for repairing defects in photomasks.

6. A method for altering the semiconductor characteristics of a semiconductor element formed on a substrate, the method comprising:

directing an energy beam at the semiconductor element, wherein the energy beam is substantially absorbed by a first portion of the semiconductor element;

thinning the semiconductor substrate under the semiconductor element; and

directing the energy beam at the first portion of the semiconductor element through the semiconductor substrate, wherein the energy beam is substantially transmitted through the semiconductor substrate.

7. The method of Claim 6, further comprising:

forming a passivation layer over the semiconductor element on the semiconductor substrate, and

mounting a support structure on the passivation layer.

8. The method of Claim 7, wherein the support structure comprises an unprocessed wafer having an oxide layer, and wherein mounting the support structure comprises covalently bonding the oxide layer of the unprocessed wafer to the passivation layer.

9. The method of Claim 7, wherein the support structure comprises a processed wafer having an oxide layer, and wherein mounting the support structure comprises covalently bonding the oxide layer of the processed wafer to the passivation layer.

10. The method of Claim 7, wherein mounting the support structure comprises using an adhesive to attach the support structure to the passivation layer.

11. The method of Claim 7, wherein thinning the backside of the processed wafer comprises a grinding operation.

12. The method of Claim 7, wherein thinning the backside of the processed wafer comprises a chemical-mechanical polishing (CMP) operation.

13. The method of Claim 7, wherein thinning the backside of the processed wafer comprises an etch process.

14. The method of Claim 6, wherein thinning the backside of the processed wafer comprises:

forming a resist layer on the backside of the processed wafer, the resist layer comprising an aperture under the transistor; and

etching the processed wafer through the aperture.

15. The method of Claim 14, wherein etching the processed wafer comprises performing an anisotropic etch process.

16. The method of Claim 14, wherein etching the processed wafer comprises performing an isotropic etch process.

17. The method of Claim 6, wherein the semiconductor substrate comprises a silicon wafer.

18. The method of Claim 6, wherein the semiconductor substrate comprises a gallium arsenide wafer.

19. The method of Claim 6, wherein the semiconductor substrate comprises an insulating plate.

20. The method of Claim 6, wherein the semiconductor substrate comprises an amorphous silicon layer.

21. The method of Claim 1, wherein the semiconductor element comprises:

a source region;

a drain region;

a channel region between the source region and the drain region;

a gate oxide formed over the channel region; and

a gate formed over the gate oxide, wherein the first portion of the semiconductor element comprises the gate, and

wherein the energy beam is substantially transmitted through the channel region.

22. The method of Claim 21, wherein the gate comprises a metal layer.

23. The method of Claim 21, wherein the gate comprises a first silicide layer.

24. The method of Claim 23, wherein the source region comprises a second silicide layer, and wherein the drain comprises a third silicide layer, the first, second, and third silicide layers being formed using a salicide process, wherein the first portion of the semiconductor element further comprises the second and third silicide layers.

25. The method of Claim 24, wherein the first, second, and third silicide layers comprise titanium silicide.

26. The method of Claim 1, wherein the semiconductor element comprises:

a first n-type region;

a p-type region formed in the n-type region;

a first contact pad formed on the first n-type region; and

a second contact pad formed on the p-type region,

wherein the first portion of the semiconductor element comprises the first contact pad and the second contact pad, and wherein the energy bean is substantially transmitted through the first n-type region and the p-type region.

27. The method of Claim 26, wherein the semiconductor element further comprises:

a second n-type region formed in the p-type region; and

a third contact pad formed on the second n-type region, wherein the first portion of the semiconductor element further comprises the third contact pad, and wherein the energy beam is substantially transmitted through the second n-type region.

28. A semiconductor structure comprising a plurality of semiconductor elements formed on a semiconductor substrate and a passivation layer formed over the plurality of semiconductor elements, each of the plurality of semiconductor elements comprising a first doped region, a second doped region, and a first element component, the semiconductor substrate having a reduced thickness at a set of the plurality of semiconductor elements formed such that the rate of heat transfer between the first element component and the first and second doped regions is substantially greater than the rate of heat transfer between the first and second doped regions and the surrounding semiconductor substrate.

29. The semiconductor structure of Claim 28, wherein the first and second doped regions of a first one of the plurality of semiconductor elements are merged into a first common region.

30. The semiconductor structure of Claim 29, wherein the source and drain regions of a second one of the plurality of semiconductor elements are merged into a second common region.

31. The semiconductor structure of Claim 28, further comprising:

a passivation layer formed over the plurality of semiconductor elements; and

a support structure mounted on the passivation layer.

32. The IC of Claim 31, wherein the support structure comprises an unprocessed wafer having an oxide layer, wherein the oxide layer is covalently bonded to the passivation layer.

33. The semiconductor structure of Claim 31, wherein the support structure comprises a processed wafer having an oxide layer, wherein the oxide layer is covalently bonded to the passivation layer.

34. The semiconductor structure of Claim 28, wherein the semiconductor substrate comprises silicon.

35. The semiconductor structure of Claim 28, wherein the semiconductor substrate comprises gallium arsenide.

36. The semiconductor structure of Claim 28, wherein the set of the plurality of semiconductor elements comprises a metal-oxide-semiconductor (MOS) transistor.

37. The semiconductor structure of Claim 36, the first doped region of the MOS transistor comprising a source region, the second doped region of the MOS transistor comprising a drain region, and the first element component of the MOS transistor comprising a gate, the MOS transistor further comprising:

a channel region between the source region and the drain region; and

a gate oxide formed over the channel region, the gate being formed over the gate oxide.

38. The semiconductor structure of Claim 37, wherein the gate comprises a first silicide layer.

39. The semiconductor structure of Claim 38, wherein the source region comprises a second silicide layer, and wherein the drain region comprises a third silicide layer, the first, second, and third silicide layers being formed by a salicide process.

40. The semiconductor structure of Claim 39, wherein the first, second, and third silicide layers comprise titanium silicide.

41. The semiconductor structure of Claim 28, wherein the set of the plurality of semiconductor elements comprises a bipolar transistor, the first doped region of the bipolar transistor comprising a collector region, the second doped region of the bipolar transistor comprising an emitter region, the bipolar transistor further comprising:

a base region formed between the collector region and the emitter region;

a first contact pad formed on the collector region;

a second contact pad formed on the emitter region; and

a third contact pad formed on the base region, the first element component of the bipolar transistor comprising the first contact pad, the second contact pad, and the third contact pad.

42. A system for programming a semiconductor element formed on a semiconductor substrate, the semiconductor element comprising a first doped region, a second doped region, and a first element component adjacent to the first doped region and the second doped region the system comprising means for directing an energy beam at the first element component through the semiconductor substrate, wherein the semiconductor substrate is substantially transparent to the energy beam and the first element component substantially absorbs the energy beam, and wherein the energy beam heats the

first element component to a temperature sufficient to cause diffusion between the first doped region and the second doped region.

43. The system of Claim 42, wherein the semiconductor element comprises a metal-oxide-semiconductor (MOS) transistor, wherein the first doped region comprises a source region, wherein the second doped region comprises a drain region, and wherein the first element component comprises a gate, wherein the MOS transistor further comprises:

a channel region formed between the source region and the drain region; and

a gate oxide formed over the channel region, the gate being formed over the gate oxide.

44. The system of Claim 43, wherein the gate comprises a metal layer.

45. The system of Claim 43, wherein the gate comprises a first silicide layer.

46. The system of Claim 45, wherein the source region comprises a second silicide layer, wherein the drain region comprises a third silicide layer, and wherein the means for directing the energy beam at the first element component comprises means for simultaneously directing the energy beam at the second and third silicide layers.

47. The system of Claim 42, wherein the semiconductor element comprises a bipolar transistor, wherein the first doped region comprises a collector region, wherein the second doped region comprises an emitter region, wherein the bipolar transistor further comprises:

a base region formed between the collector region and the emitter region;

a first contact pad formed over the base region;

a second contact pad formed over the collector region; and

a third contact pad formed over the emitter region, wherein the first element component comprises the first contact pad.

48. The system of Claim 47, wherein the means for directing the energy beam at the first element component comprises means for simultaneously directing the energy beam at the second and third contact pads.

49. The system of Claim 42, wherein the means for directing the energy beam at the first element component comprises a CO_2 laser.

50. The system of Claim 42, wherein the means for directing the energy beam at the first element component comprises a YAG laser.

51. The system of Claim 42, wherein the means for directing the energy beam at the first element component comprises a laser ablation system for repairing defects in photomasks.